

Substitute for Form 1449/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(use as many sheets as necessary)</i>				Application Number	10/627,333
				Filing Date	July 24, 2003
				First Named Inventor:	Terrence Anthony Staton
				Art Unit	2857
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket Number	2998.P033
<b>NON PATENT LITERATURE DOCUMENTS</b>					
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T <sup>2</sup>
JCC		ABHIK ROYCHOUDHURY et al., "Using formal techniques to Debug the AMBA System-on-Chip Bus Protocol", School of Computing National University of Singapore, Singapore 117543, {abhik, tulika, karrisid}@comp.nus.edu.sg, prior to filing date of this application, pp.6 total.			
JCC		SONICST <sup>TM</sup> SMART IP for Greater SOC Complexity Faster, Synapse 3220, "Synapse 3220 <sup>TM</sup> SMART Interconnect IP <sup>TM</sup> ", www.sonicsinc.com/sonics/products/synapse 3220, May 30, 2003, pp.1-2.			
JCC		THOMAS ANDERSON, Co-Chair, VSIA Functional Verification DWG, "Verification Reuse for Embedded Virtual Components", 0-IN Design Automation, VSI Alliance <sup>TM</sup> , March 4, 2002, pp. 1-23.			
JCC		TOM ANDERSON, VP of Applications Engineering 0-In Design Automation, Inc., Co-Chair, VSIA Functional Verification DWG, tla@0-in.com, "Verification: Reuse It or Lose It", 0-IN Design Automation, DesignCon 2002, pp. 1-48.			

Examiner Signature		Date Considered	5/30/06
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\*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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